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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,118	11/18/2003	Katsumi Shibayama	046124-5179	2756

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,118	SHIBAYAMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/2004 and 08/1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Japanese provisional Application Nos. P2002-334326 filed 18/11/2002 and Prov. 60/430620 filed on 04/12/2002 which papers have been placed of record in the file.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-16 , drawn to a back illuminated photodiode , classified in class 378, subclass 19+.

II. Claims 17 to 19 , drawn to a semiconductor device , classified in class 257, subclass 465.

III. Claims 20 -25, drawn to a manufacturing method for back illuminated photo diode , classified in class 438, subclass 160 +.

Inventions Gr. I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the sub combination as claimed includes a

The subcombination has separate utility such as the photodiode can be used in as light emitting device whereas the combination (semiconductor device) can be used as a switch.

Inventions II and III are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

In the instant case the process as claimed can be used to make other and materially different product namely a LCD or semiconductor instead of photodiode .

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II or III, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. John Smith on December 07, 2004 a provisional election was made without traverse to prosecute the invention of Gr. I , claim 1-16

. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 17- 25 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statements (PTO-1449) filled on Mrch12,2004 and August 20, 2004 .

The references on PTO 1499s submitted on 3/12/04 and 08/20/04 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Drawings

The drawings filed on November 18, 2003 have been accepted by the draftsperson (see attached PTO-948)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991, herein after Mattson) and in view of Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo)

With respect to claim 1 Mattson describes a back illuminated photodiode array comprising ; a first conductive type semiconductor substrate having a light-incident surface (Mattson figure 7 #64, fig. 12 # 142 , abstract 4 th line from bottom).

Mattson describes an opposite surface but does not specifically mention a plurality of recessed portions located opposite said light incident surface.

However Chappo a patent from the same filed of endeavor describes in 10, etc. #120 and col. 11 lines 4-8 describe an opposite surface with a plurality of recessed portions located opposite said light-incident surface to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other .

Therefore it would have been obvious t o one of ordinary skill in the art at the time of the invention to include the an opposite surface with a plurality of recessed portions located opposite said light-incident surface instead of Mattson's opposite surface in Mattson's device. The motivation to make the afore mentioned substitution is to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other. (Chappo 2 lines 51-67 and col. 3 lines 1-12).

The remaining limitations of claim 1 are :

a plurality of second conductive type semiconductor regions spatially detached at each bottom of said recessed portions; (Chappo col. 11 lines 5-8) wherein said semiconductor regions individually constitute pn junctions together with said semiconductor substrate. (Mattson figure 3 , Chappo col. 8 line 50-55)

With respect to claim 2 Mattson describes a back illuminated photodiode array according to claim 1, wherein said semiconductor substrate regions between a plurality of said recessed portions constitute a frame part which is thicker than said recessed portions. (Chappo figure 15 and col. 12 lines 27-34.).

With respect to claim 3 Mattson describes a back illuminated photodiode array according to claim 1, wherein said semiconductor substrate is composed of a single semiconductor substrate. (Chappo Figure 2 A# 52, col. 6 lines6-8).

With respect to claim 4 Mattson describes a back illuminated photodiode array according to claim 1, wherein said semiconductor substrate is provided with a first semiconductor substrate having said light-incident surface and a second semiconductor substrate bonded to sald first semiconductor substrate and having side walls of said recessed portions. (Chappo col. 6 lines47-49, fig. 10 #col. 11 lines 3-7).

With respect to claim 5 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an etching stop layer existing between said first semiconductor substrate and said second semiconductor substrate and having resistance to a specific etching agent to be used for said second semiconductor substrate. (Mattson col. 5 lines 8-9, and Chappo col.6 lines 6-15, it is inherent for a stop

layer to resistant the etching agent for second substrate in oder for the stop layer to function as a stop layer) .

With respect to claim 6 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate. (Chappo col. 7 lines 23-31, Mattson col.5 lines 24-25).

With respect to claim 7 Mattson describes a back illuminated photodiode array according to claim 2, comprising a plurality of electrode pads formed on each top surface of said frame part and individually and electrically connected to said semiconductor regions. (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48 , figures 2 and 6).

With respect to claim 8 Mattson describes a back illuminated photodiode array according to claim 7, further comprising: an electric insulation layer formed on said frame part; ((Chappo col. 7 lines 23-31, Mattson col.5 lines 24-25)and a conductive member formed on said electric insulation layer and connecting electrically said semiconductor regions with said electrode pads. (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48 , figures 2 and 6).

With respect to claim 9 Mattson describes a back illuminated photodiode array according to claim 8, wherein said electric insulation layer is provided with a contact hole for connecting an end of said conductive member to said semiconductor regions. (Chappo figure 10).

With respect to claim 10 Mattson describes a back illuminated photodiode array according to claim 2, where In said semiconductor regions extend from said bottoms to side surfaces of said recessed portions. (Chappo figure 10, col.11 line5-7).

With respect to claim 11 Mattson describes a back illuminated photodiode array according to claim 2: wherein said semiconductor regions extend from said bottoms over side surfaces of said recessed portions to a top surface of said frame part. (Chappo figure 9, col. 9 lines 60 –col. 10 line 20).

With respect to claim 12 Mattson describes a back illuminated photodiode array according to claim 11, comprising: an electric insulation layer formed on said frame part and having a contact hole opposing said top surface; and electrode pads electrically connected to said semiconductor regions through said contact hole. (Chappo figure 10, col. 10 line 30- col. 11 line 7).

With respect to claim 13 Mattson describes a back illuminated photodiode array according to claim 2, wherein said frame part is provided with a first conductive type separation region higher in impurity concentration than said semiconductor substrate.(Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped , the first conductive type separation region has higher impurity concentration than the substrate) .

With respect to claim 14 Mattson describes a back illuminated photodiode array according to claim I wherein an opening size of said recessed portions decreases with

an increase in the depth of said recessed portions.(well known in the art to decreasing recessed protion).

With respect to claim 15 Mattson describes a back illuminated photodiode array according to claim 1, wherein said light-incident surface side of said semiconductor substrate is provided with a first conductive type accumulation layer which is higher in impurity concentration than said semiconductor substrate. (Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped , the first conductive type separation region has higher impurity concentration than the substrate and fig. 14 ,vias and conductive type accumulation layer on first surface and col.12 lines22-25).

B. Claim 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991, herein after Mattson) and Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo) as applied to claims 1-13 and 15 above and further in view of Yamanaka et al. (U.S Patent No. 6,372,558, herein after Yamanaka).

With respect to claim 16 Mattson describes a back illuminated photodiode array according to claim 4, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation.

Matson and Chappo describe a back illuminated photodiode array according to claim 4 but do not specifically describe the first and the second semiconductor substrates to be in different in their crystal plane orientation.

However, Yamanaka in figure 8A and col. 13 line 60- col. 14 line 20 describes the first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yamanaka's the first and the second semiconductor substrates to be in different in their crystal plane orientation In Chappo's device to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The (571) 272-1718 examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

December 13, 2004